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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,563	06/19/2003	Lawrence C. Gunn III	LUX-P003	6066

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EXAMINER	
DICKEY, THOMAS L	
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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/600,563	GUNN ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10,12-39,42-49,51-61 and 63-73* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,9,12,14-18,21,28,34,38,44-46,49,51,53-57,60 and 69-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/23/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 6-8,10,13,19,20,22-27,29-33,35-37,39,42,43,47,48,52,58,59,61,63-68,72 and 73.

DETAILED ACTION

1. The amendment filed on 04/16/2008 has been entered.

Information Disclosure Statement

2. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Election/Restriction

3. Applicant's election with traverse of Species 8 (as described in words and figures in figure 8, and paragraphs 0048-0058) in the reply filed on 04/16/2008 is acknowledged.

Applicant has stated that all pending claims "are directed to" the elected embodiment. However, only claims that (when properly construed) read on[1] the elected embodiment may be considered after election.

Claims 6, 7, and 47 require a dielectric component of a transistor selected from a group comprising an inter-layer dielectric film, a gate spacer, a silicide block, a dielectric

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[1] Note that "A claim reads on something, if every element of that claim is present in that which it reads on." See http://www.delphion.com/help/glossary#readon. "Read on" has the same meaning regardless of whether it is used to determine infringement, anticipation, obviousness, new matter issues, or restrictability, The phrase "read on" is often used by patent professionals. The examiner cites Delphion's definition because it appears representative of the common understanding of patent professionals.

spacer, a passivation film, an isolation dielectric and a field oxide. The elected embodiment does not include a dielectric component of a transistor selected from a group comprising an inter-layer dielectric film, a gate spacer, a silicide block, a dielectric spacer, a passivation film, an isolation dielectric and a field oxide. Claims 6, 7, and 47 does not read on the elected embodiment because the elected embodiment does not include a dielectric component of a transistor selected from a group comprising an inter-layer dielectric film, a gate spacer, a silicide block, a dielectric spacer, a passivation film, an isolation dielectric and a field oxide. Because claims 6, 7, and 47 does not read on the elected embodiment, claims 6, 7, and 47 are withdrawn from consideration.

Claims 8 and 48 require a substrate is selected from the group comprising: silicon on insulator (SOI), silicon on sapphire (SOS) and a silicon membrane (also known as silicon on nothing, SON). The elected embodiment does not include a substrate is selected from the group comprising: silicon on insulator (SOI), silicon on sapphire (SOS) and a silicon membrane (also known as silicon on nothing, SON). Claims 8 and 48 do not read on the elected embodiment because the elected embodiment does not include a substrate is selected from the group comprising: silicon on insulator (SOI), silicon on sapphire (SOS) and a silicon membrane (also known as silicon on nothing, SON). Because claims 8 and 48 do not read on the elected embodiment, claims 8 and 48 are withdrawn from consideration.

Claim 10 requires an integrated circuit selected from the group comprising a CMOS integrated circuit, a BiCMOS integrated circuit and a bipolar junction integrated circuit. The elected embodiment does not include an integrated circuit selected from the group comprising a CMOS integrated circuit, a BiCMOS integrated circuit and a bipolar junction integrated circuit. Claim 10 does not read on the elected embodiment because the elected embodiment does not include an integrated circuit selected from the group comprising a CMOS integrated circuit, a BiCMOS integrated circuit and a bipolar junction integrated circuit. Because claim 10 does not read on the elected embodiment, claims 10 and 50 are withdrawn from consideration.

Claims 13 and 52 require a conductive plug formed simultaneously with a metal layer. The elected embodiment does not include a conductive plug formed simultaneously with a metal layer. Claims 13 and 52 do not read on the elected embodiment because the elected embodiment does not include a conductive plug formed simultaneously with a metal layer. Because claims 13 and 52 do not read on the elected embodiment, claims 13 and 52 are withdrawn from consideration.

Claims 19 and 58 require a local interconnection comprised of a material selected from the group comprising tungsten and aluminum. The elected embodiment does not include a local interconnection comprised of a material selected from the group comprising tungsten and aluminum. Claims 19 and 58 do not read on the elected

embodiment because the elected embodiment does not include a local interconnection comprised of a material selected from the group comprising tungsten and aluminum. Because claims 19 and 58 do not read on the elected embodiment, claims 19 and 58 are withdrawn from consideration.

Claims 20, 59, and 72 require an element on an integrated circuit selected from the group comprising a capacitor, a resistor, an inductor, a diode, a transistor and a bond pad. The elected embodiment does not include an element on an integrated circuit selected from the group comprising a capacitor, a resistor, an inductor, a diode, a transistor and a bond pad. Claims 20, 59, and 72 do not read on the elected embodiment because the elected embodiment does not include an element on an integrated circuit selected from the group comprising a capacitor, a resistor, an inductor, a diode, a transistor and a bond pad. Because claims 20, 59, and 72 do not read on the elected embodiment, claims 20, 59, and 72 are withdrawn from consideration.

Claims 22-27, 61, 63, 64, and 73 require a plurality of dopants in the silicon of a heterojunction or a plurality of dopants in the germanium of the heterojunction. The elected embodiment does not include a plurality of dopants in the silicon of a heterojunction or a plurality of dopants in the germanium of the heterojunction. Claims 22-27, 61, 63, 64, and 73 do not read on the elected embodiment because the elected embodiment does not include a plurality of dopants in the silicon of a heterojunction or a

plurality of dopants in the germanium of the heterojunction. Because claims 22-27, 61, 63, 64, and 73 do not read on the elected embodiment, claims 22-27, 61, 63, 64, and 73 are withdrawn from consideration.

Claim 29 requires a silicon waveguide with an input and an output. The elected embodiment does not include a silicon waveguide with an input and an output. Claim 29 does not read on the elected embodiment because the elected embodiment does not include a silicon waveguide with an input and an output. Because claim 29 does not read on the elected embodiment, claim 29 is withdrawn from consideration.

Claims 30-33 and 65-68 require a mode converter with an input and an output. The elected embodiment does not include a mode converter with an input and an output. Claims 30-33 and 65-68 do not read on the elected embodiment because the elected embodiment does not include a mode converter with an input and an output. Because claims 30-33 and 65-68 do not read on the elected embodiment, claims 30-33 and 65-68 are withdrawn from consideration.

Claims 35 and 69 require a CMOS transistor selected from the group of transistors comprising a fully depleted CMOS transistor, a partially depleted CMOS transistor, a floating body CMOS transistor and a body tied CMOS transistor. The elected embodiment does not include a CMOS transistor selected from the group of transistors comprising a fully depleted CMOS transistor, a partially depleted CMOS transistor, a

floating body CMOS transistor and a body tied CMOS transistor. Claims 35 and 69 do not read on the elected embodiment because the elected embodiment does not include a CMOS transistor selected from the group of transistors comprising a fully depleted CMOS transistor, a partially depleted CMOS transistor, a floating body CMOS transistor and a body tied CMOS transistor. Because claims 35 and 69 do not read on the elected embodiment, claims 35 and 69 are withdrawn from consideration.

Claim 38 requires a combination of “an optical input” and “inputs for receiving optical signals”. The elected embodiment does not include a combination of “an optical input” and “inputs for receiving optical signals”. Claim 38 does not read on the elected embodiment because the elected embodiment does not include a combination of “an optical input” and “inputs for receiving optical signals”. Because claim 38 does not read on the elected embodiment, claim 38 is withdrawn from consideration.

Claims 39 and 70 require a data structure representation. The elected embodiment does not include a data structure representation. Claims 39 and 70 do not read on the elected embodiment because the elected embodiment does not include a data structure representation. Because claims 39 and 70 do not read on the elected embodiment, claims 39 and 70 are withdrawn from consideration.

Claims 42 and 43 require a plurality of maskworks. The elected embodiment does not include a plurality of maskworks. Claims 42 and 43 do not read on the elected

embodiment because the elected embodiment does not include a plurality of maskworks. Because claims 42 and 43 do not read on the elected embodiment, claims 42 and 43 are withdrawn from consideration.

Claim Objections

4. Claims 11 and 50 are objected to because of the following informalities:

Applicant lists the status of claims 11 and 50 "cancelled." However, and contrary to rule, Applicant lists text for these claims. Cancelled claims should not list any text. "No claim text shall be presented for any claim in the claim listing with the status of "canceled" or "not entered." 37 CFR 1.121(c)(4)(i).

Appropriate correction (a new claim set which does not list text for any cancelled claim) is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 60 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was

not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant's originally filed application does not reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the invention claimed in claim 60, including the "COMS integrated circuit" recited in line 9.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 51-58 and 60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 51-58, it is noted that claim 51 does not end in a period. The scope of claim 51 (and claims 52-58, which incorporate claim 51) is therefore indeterminate, and the resultant claims 51-58 are narrative in form. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative

device. The claim(s) must be in one sentence form only. Note the format of the claims in the patent(s) cited.

Correction is required.

Claim 60 recites the limitation "the CMOS integrated circuit" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5, 9, 12, 14-18, 21, 28, 34, 38, 44-46, 49, 51, 53-57, 60 and 69-71 are rejected under 35 U.S.C. § 102(b) as being anticipated by DELWALA (2002/0172464).

A. With regard to claims 5 and 9 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium on silicon heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-

5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein the cladding 104-5109 further comprises a bottom cladding 104 comprised of the insulating layer of an SOI 152 that also serves as the substrate of a CMOS integrated circuit 5101, a side cladding 5109 and a top cladding, where each of the claddings is comprised of a plurality of dielectric materials, wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claims 5 and 9 do not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in

the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a "product by process" claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1100. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

> [Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its

> method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

B. With regard to claims 12, 14-18, and 34, Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium on silicon heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole

pairs caused by photons absorbed in the depletion region, wherein each of the second plurality of conductive contacts 118,122 comprises a metal silicide ohmic contact to the silicon layer 191 of the heterojunction, and a tungsten conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44) and the conductive plug 5121 is formed simultaneously with the metal layer 5120, further comprising the fabrication of an ohmic contact on the source, drain, body, or gate of a CMOS transistor 8101 at the same time as the fabrication of an ohmic contact on the silicon of the heterojunction; the fabrication of a conductive plug 5121 to an ohmic contact of a transistor 8101 at the same time as the fabrication of the conductive plug 5121 to an ohmic contact to the silicon of the heterojunction, and the fabrication of a local interconnection between a pair of transistors 8101-9101, at the same time as fabricating a local interconnection for coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors 8101-9101, wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claims 12, 14-18, and 34 do not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon

layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

C. With regard to claim 21 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium on silicon heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein each of the first plurality of conductive contacts 120 comprises an ohmic contact to the germanium of the heterojunction, and a conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44), wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 21 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims

or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

D. With regard to claim 28 Delwala discloses a waveguide photodetector comprising a waveguide 160 and an input to the waveguide 160, the waveguide 160 comprising a core 190 comprised of a germanium on silicon heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium on silicon heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 28 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the

waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

E. With regard to claim 38 Delwala discloses a semiconductor chip comprising a germanium on silicon waveguide photodetector located on the semiconductor chip, said germanium on silicon waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium on silicon heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, and a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials; an optical input; a first plurality of conductive contacts 120 coupled to said germanium layer 108; and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191; and, inputs for receiving optical signals; outputs for outputting electrical signals; and a semiconductor device comprising a CMOS transistor 8101 connected to the germanium on silicon waveguide photodetector outputs and located on the semiconductor chip. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

F. With regard to claim 44 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108 and not coupled to the silicon 191; a second plurality of conductive contacts 118,122 (800 in fig. 43)

coupled to the silicon 191 and not coupled to the germanium 108, and wherein said first plurality of conductive contacts 120 are displaced from said second plurality of conductive contacts 118,122; and, a CMOS transistor body 8108-8114-8110. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 44 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon of the heterojunction, because only the final product is relevant, not the recited process of fabricating the CMOS transistor body at the same time as the fabrication of the silicon of the heterojunction. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not

the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

G. With regard to claim 45 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, and a cladding 104-5109 comprised of a plurality of dielectric materials; and, a first plurality of conductive contacts 120 coupled to the germanium 108; and, a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191, wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 45 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming

at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp*., 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

H. With regard to claims 46 and 49 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on

silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric materials; a first plurality of conductive contacts 120 coupled to the germanium 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191; wherein the cladding 104-5109 comprises a bottom cladding 104 comprised of the insulating layer of an SOI 152 that also serves as the substrate of a CMOS integrated circuit 5101, a side cladding 5109 and a top cladding, wherein at least one conductive contact of the first plurality of conductive contacts 120 and the second plurality of conductive contacts 118,122 is operatively coupled to a CMOS transistor 8101, and wherein at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide are formed from a starting silicon layer. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claims 46 and 49 do not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

I. With regard to claims 51 and 53-57 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191, wherein each of the second plurality of conductive contacts 118,122 comprises a metal silicide ohmic contact to the silicon of the heterojunction, and a tungsten

conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of a CMOS integrated circuit 5101, and further comprising an ohmic contact on the source, drain, body, or gate of a transistor 8101; an ohmic contact on the silicon of the heterojunction; a conductive plug 5121 to an ohmic contact of a transistor 8101; a conductive plug 5121 to an ohmic contact to the silicon of the heterojunction, a local interconnection between a pair of transistors 8101-9101, and a local interconnection coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors 8101-9101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claims 51 and 53-57 do not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited processes of fabricating the ohmic contact on the source, drain, body, or gate of a transistor 8101 at the same time as fabricating the ohmic contact on the silicon of the heterojunction and fabricating the conductive plug 5121 to an ohmic contact of a transistor; fabricating the conductive plug to an ohmic contact of the transistor at the same time as fabricating the conductive plug 5121 to an ohmic contact to the silicon of the heterojunction and fabricating the of a local interconnection between a pair of transistors; fabricating the local interconnection between a pair of transistors at the

same time as fabricating the local interconnection for coupling the ohmic contact on the silicon of the heterojunction with the ohmic contact on one of the transistors; and forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

J. With regard to claim 60 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108 wherein each of the first plurality of conductive contacts 120 comprises an ohmic contact to the germanium of the heterojunction, and a conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of a COMS integrated circuit 5101, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 60 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

K. With regard to claim 71 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of electrical contacts 120 coupled to the germanium 108; a second plurality of electrical contacts 118,122 coupled to the silicon 191; and, a CMOS transistor body 8108-8114-8110 fabricated at the same time as the fabrication of the silicon of the heterojunction and wherein the transistor body 8108-8114-8110 is external to the

waveguide 160 and displaced from the waveguide 160. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

The applicant's claim 71 does not distinguish over the Delwala reference regardless of the process used to form the CMOS transistor and the silicon layer of the core of the waveguide, because only the final product is relevant, not the recited process of forming at least a portion of the CMOS transistor and the silicon layer of the core of the waveguide by starting with a starting silicon layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new

method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Response to Arguments

8. Applicant's arguments with respect to claims 5, 9, 12, 14-18, 21, 28, 34, 38, 44-46, 49, 51, 53-57, 60 and 69-71 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L Dickey/
Primary Examiner, Art Unit 2826